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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/844,958	04/27/2001	Milton J. Boden JR.	IR-2048 Div (2-2637)	1815

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EXAMINER
TRAN, THIEN F

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/844,958	Applicant(s) BODEN, MILTON J.	
	Examiner Thien Tran	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-35,39 and 41-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *41-46* is/are allowed.

6)☒ Claim(s) *30-35 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claim 31 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The limitation "wherein the thickness of said gate dielectric is chosen to optimize resistance to high radiation effects and wherein the thickness of said bottom dielectric is chosen to optimize resistance to SEE" is already recited in parent claim 39.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 30-33 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cogan et al. (USPN 5,298,781) in view of Floyd et al. (USPN 5,917,216) and Harada (USPN 5079,602).

Cogan et al. discloses a trench MOS gated device (Fig. 2) comprising a silicon wafer (102, 104) of one conductivity type (n-type) having a plurality of spaced shallow active trenches 111 containing respective gate structures; each of said active trenches having partly vertical walls joined at their bottoms by respective trench bottoms; each of said active trenches containing a gate structure having a gate dielectric 112b on

portions of its said vertical walls, a bottom dielectric 112a on the bottom and a conductive polysilicon plug as a gate electrode 114 contacting the interior surface of the gate dielectric 112b; a channel region 106 of opposite conductivity type (p-type) and an upper source region 108 comprising a diffusion; and a common source contact 110 contacting each of said source regions (108, 108a-108d); a common gate electrode 114 connected to each of said conductive plugs (114a, 114) in each of said active trenches containing a gate structure and a drain contact 118 connected to a drift region beneath said active trenches. Cogan et al. does not disclose the polysilicon gate electrode 114 being doped of n-type. However, it is well known in the art to have the polysilicon gate electrode doped of n-type as shown for example by Floyd et al. (see Fig. 1a) in order to increase the gate electrode conductivity. Therefore, forming the polysilicon gate electrode 114 of n-type impurity would have been obvious modification. Cogan et al. does not disclose a plurality of intermediate trenches each disposed between a respective pair of active trench gate structures. Harada discloses a plurality of intermediate trenches 14 each disposed between a respective pair of active gate structures (Fig. 8) wherein each of the intermediate trenches has partly vertical walls and trench bottom, each of the intermediate trenches having a shallow diffusion 16 of p-type extending from its walls and bottom and being filled with a conductive polysilicon plug 17 of p-type. Both Cogan et al. and Harada teach a vertical type MOS device, it would have been obvious to have the intermediate trench with a shallow diffusion of p-type extending from its walls and bottom and being filled with a conductive polysilicon plug of p-type in Cogan et al. to improve the current capacity of the device. As a result,

a plurality of intermediate trenches each disposed between a respective pair of active trench gate structures are formed, wherein each of the intermediate trenches has partly vertical walls and trench bottom, each of the intermediate trenches having a shallow diffusion of p-type extending from its walls and bottom and being filled with a conductive polysilicon plug of p-type in contact with source regions.

Cogan et al. further discloses the gate dielectric 112b and the bottom dielectric 112a formed of silicon dioxide, wherein the gate dielectric 112b has a thickness of 100 to 2500 angstroms and the bottom dielectric 112a has a thickness of 500-5000 angstroms. Assuming less than 900 angstrom is selected, the gate dielectric 112b has the claimed thickness; and assuming thickness of greater than 1300 angstrom is selected, the bottom dielectric 112a has the claimed thickness.

The modified Cogan et al. has the claimed structure with a thin gate dielectric and a thick bottom dielectric having the claimed ranges (assuming the thickness of the gate dielectric and the thickness of the bottom dielectric are chosen within the disclosed ranges to have the same thicknesses as claimed); it is inherent that the structure of the modified Cogan et al. has improved resistance to both high radiation and single event high energy charged particles (SEE) and resistance to high radiation effects and resistance to SEE are optimized.

Regarding claims 30 and 33, source regions (108, 108a-108d) between said active and intermediate trenches are of n-type.

Regarding claim 32, active trenches 111 are parallel elongated trenches.

Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cogan et al. (USPN 5,298,781) in view of Floyd et al. (USPN 5,917,216) and Harada (USPN 5,079,602) as applied to claim 39, and further in view of Bulucea et al. (USPN 5,298,442).

The modified Cogan et al. does not disclose the active trenches containing gated structures are polygonal in topology and are symmetrical spaced and disposed over the surface of the silicon wafer wherein the source regions surrounding the at least a plurality of the active trenches. Bulucea et al. discloses vertical MOS device (Fig. 8) comprising active trenches 29 containing gated structures being polygonal in topology and symmetrical spaced and disposed over the surface of the wafer wherein the source regions 28 surrounding the at least a plurality of the active trenches. It would have been obvious to a person having ordinary skill in the art at hen time the invention was made to form the modified structure of Cogan et al. having the active trenches 111 containing gated structures being polygonal in topology and symmetrical spaced and disposed over the surface of the wafer wherein the source regions 108 surrounding the at least a plurality of the active trenches as taught by Bulucea et al. in order to suppress voltage breakdown near the gate. As a result, the intermediate trenches surrounding the at least a plurality of the active trenches consisting of a trench of lattice shape in polygon.

Regarding claim 35, source regions (108, 108a-108d) between said active and intermediate trenches are of n-type.

Allowable Subject Matter

Claims 41-46 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien Tran whose telephone number is (703) 308-4108. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

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August 24, 2003

Thien Tran
Patent Examiner
Technology Center 2800